VNQ830PEP-E

Quad channel high side driver

Features

Type	$R_{DS(on)}$	I_{OUT}	V_{CC}
VNQ830PEP-E	60mΩ[1]	14A[1]	36V

1. Per each channel.

- CMOS compatible inputs
- Open drain status outputs
- On-state open load detection
- Off-state open load detection
- Shorted load protection
- Undervoltage and overvoltage shutdown
- Loss of ground protection
- Very low standby current
- Reverse battery protection[a]
- In compliance with the 2002/95/EC european directive



PowerSSO-24

Description

The VNQ830PEP-E is a monolithic device made using STMicroelectronics VIPower™ M0-3 Technology. The VNQ830PEP-E is intended for driving any type of multiple load with one side connected to ground.

The Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table).

Active current limitation combined with thermal shutdown and automatic restart protects the device against overload. The device detects the open load condition in both the on and off-state.

In the off-state the device detects if the output is shorted to V_{CC}. The device automatically turns off in the case where the ground pin becomes disconnected.

a. See *Application schematic on page 16*

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-24	VNQ830PEP-E	VNQ830PEPTR-E

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1 Block diagram and pin description

Figure 1. Block diagram

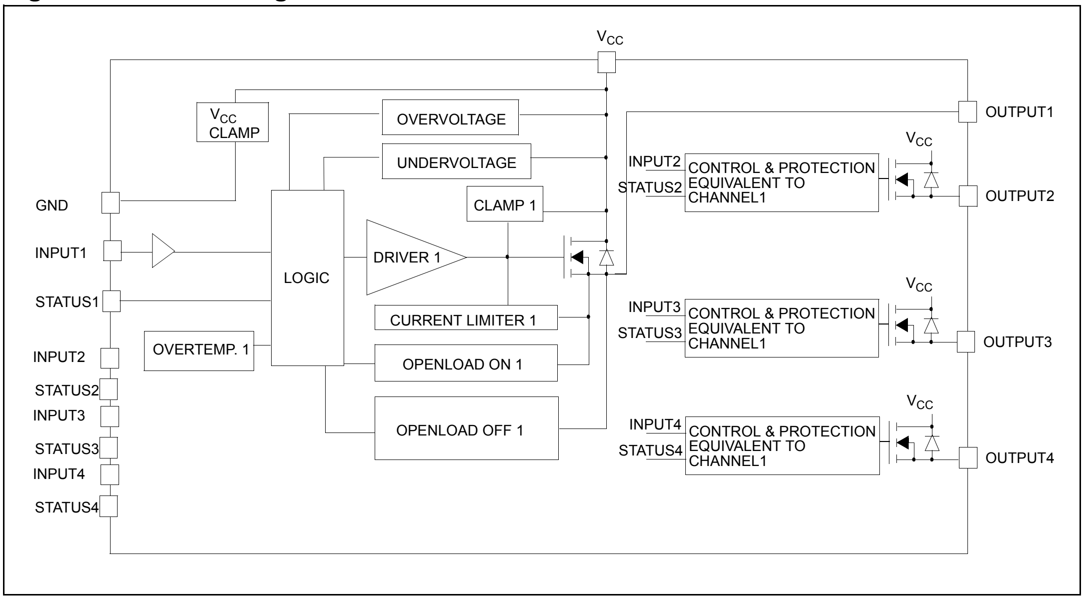


Figure 2. Configuration diagram (top view)

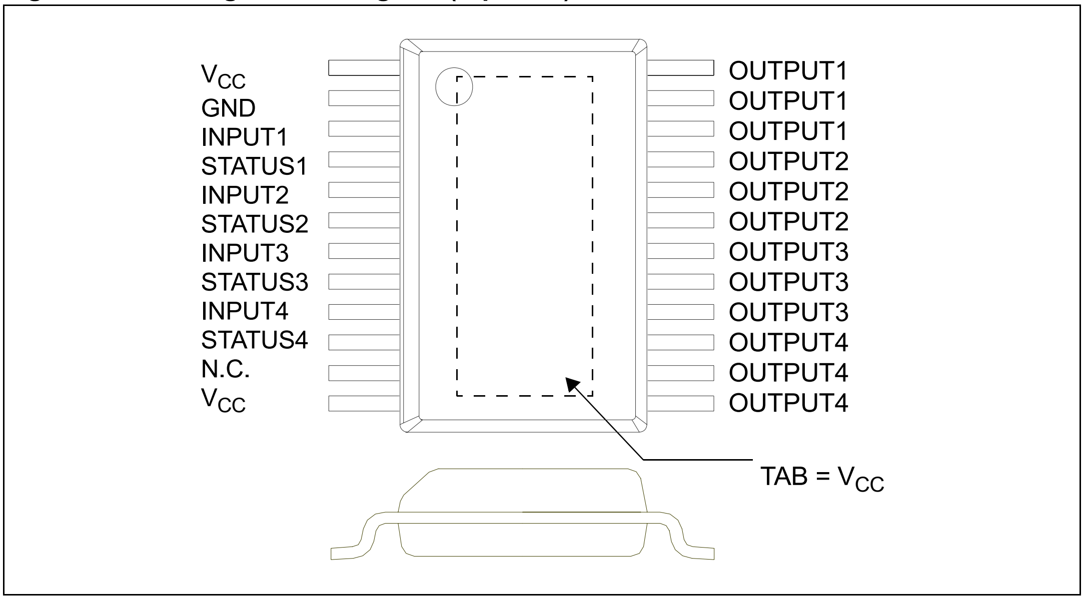


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Status	N.C.	Output	Input
Floating	X	X	X	X
To ground		X		Through 10KΩ resistor

2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
- V_{CC}	Reverse DC supply voltage	- 0.3	V
- I_{GND}	DC reverse ground pin current	- 200	mA
I_{OUT}	DC output current	Internally limited	A
- I_{OUT}	Reverse DC output current	- 12	A
I_{IN}	DC input current	+/- 10	mA
I_{STAT}	DC Status current	+/- 10	mA
V_{ESD}	Electrostatic discharge (human body model: R=1.5KΩ; C = 100pF) – Input – Status – Output – V_{CC}	 4000 4000 5000 5000	 V V V V
P_{tot}	Power dissipation (per island) at T_{lead} = 25°C	83	W
T_j	Junction operating temperature	Internally limited	°C
T_c	Case operating temperature	- 40 to 150	°C
T_{stg}	Storage temperature	- 55 to 150	°C

2.2 Thermal data

Table 4. Thermal data (per island)

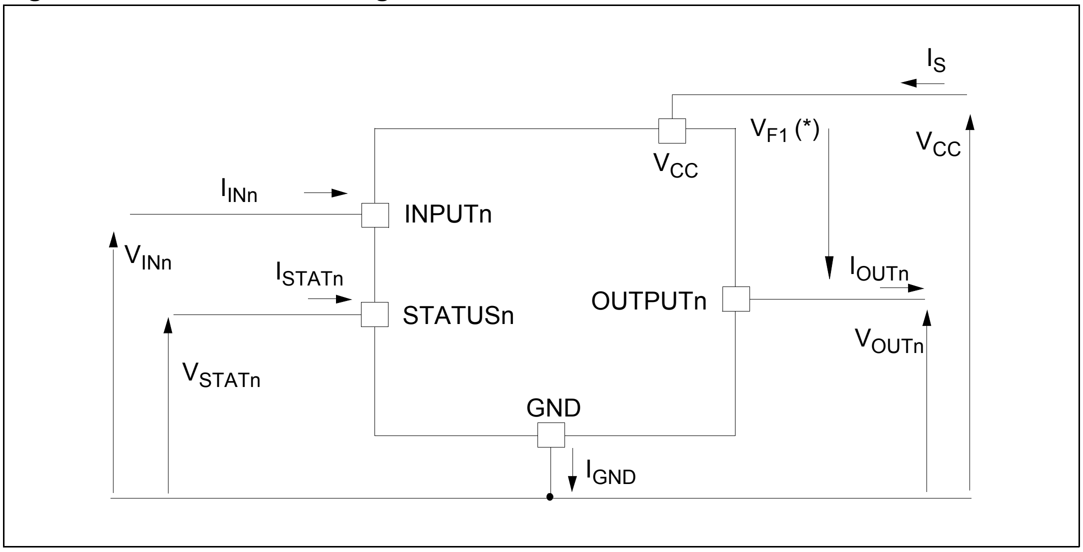
Symbol	Parameter	Value		Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	1.5		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (one chip ON)	56[(1)]	41.7[(2)]	°C/W

1. When mounted on a standard single-sided FR-4 board with 0.5cm^2 of Cu (at least 35 µm thick). Horizontal mounting and no artificial air flow.
2. When mounted on a standard single-sided FR-4 board with 8cm^2 of Cu (at least 35 µm thick). Horizontal mounting and no artificial air flow.

2.3 Electrical characteristics

Values specified in this section are for 8V < V_{CC} < 36V; -40°C < T_j < 150°C, unless otherwise stated.

Figure 3. Current and voltage conventions



Note: $V_{Fn} = V_{CCn} - V_{OUTn}$ during reverse battery condition.

Table 5. Power output

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		5.5	13	36	V
V_{USD}	Undervoltage shutdown		3	4	5.5	V
V_{OV}	Overvoltage shutdown		36			V
R_{ON}	On-state resistance	I_{OUT} = 2A; T_j = 25°C I_{OUT} = 2A; V_{CC} > 8V			65 120	mΩ mΩ
I_S	Supply current	Off-state; V_{CC} = 13V; $V_{IN} = V_{OUT}$ = 0V Off-state; V_{CC} = 13V; $V_{IN} = V_{OUT}$ = 0V; T_j = 25°C On-state; V_{CC} = 13V; V_{IN} = 5V; I_{OUT} = 0A		20 20 8.5	60 40 13.5	µA µA mA
$I_{L(off1)}$	Off-state output current	$V_{IN} = V_{OUT}$ = 0V	0		50	µA
$I_{L(off2)}$	Off-state output current	V_{IN} = 0V; V_{OUT} = 3.5V	-75		0	µA

Table 5. Power output (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{L(off3)}$	Off-state output current	$V_{IN} = V_{OUT} = 0V$; $V_{CC} = 13V$; $T_j = 125°C$			5	µA
$I_{L(off4)}$	Off-state output current	$V_{IN} = V_{OUT} = 0V$; $V_{CC} = 13V$; $T_j = 25°C$			3	µA

Table 6. Protections

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		135			°C
T_{hyst}	Thermal hysteresis		7	15		°C
t_{SDL}	Status delay in overload conditions	$T_j > T_{TSD}$			20	µs
I_{lim}	Current limitation	$V_{CC} = 13V$ $5.5V < V_{CC} < 36V$	14	18	23 23	A A
V_{demag}	Turn-off output clamp voltage	$I_{OUT} = 2A$; $L = 6mH$	V_{CC} - 41	V_{CC} - 48	V_{CC} - 55	V

Note: To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 7. V_{CC} - output diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_F	Forward on voltage	$- I_{OUT} = 1.3A$; $T_j = 150°C$	-	-	0.6	V

Table 8. Switching ($V_{CC} = 13V$; $T_j = 25°C$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 6.5\Omega$ from V_{IN} rising edge to $V_{OUT} = 1.3V$ (see *Figure 5*)	-	30	-	µs
$t_{d(off)}$	Turn-off delay time	$R_L = 6.5\Omega$ from V_{IN} falling edge to $V_{OUT} = 11.7V$ (see *Figure 5*)	-	30	-	µs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	$R_L = 6.5\Omega$ from $V_{OUT} = 1.3V$ to $V_{OUT} = 10.4V$ (see *Figure 5*)	-	See *Figure 10*	-	V/µs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	$R_L = 6.5\Omega$ from $V_{OUT} = 11.7V$ to $V_{OUT} = 1.3V$ (see *Figure 5*)	-	See *Figure 12*	-	V/µs

Table 9. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level				1.25	V
I_{IL}	Low level input current	V_{IN} = 1.25V	1			µA
V_{IH}	Input high level		3.25			V
I_{IH}	High level input current	V_{IN} = 3.25V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.5			V
V_{ICL}	Input clamp voltage	I_{IN} = 1mA I_{IN} = -1mA	6	6.8 - 0.7	8	V V

Table 10. Status pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{STAT}	Status low output voltage	I_{STAT} = 1.6mA			0.5	V
I_{LSTAT}	Status leakage current	Normal operation; V_{STAT} = 5V			10	µA
C_{STAT}	Status pin input capacitance	Normal operation; V_{STAT} = 5V			100	pF
V_{SCL}	Status clamp voltage	I_{STAT} = 1mA I_{STAT} = - 1mA	6	6.8 - 0.7	8	V V

Table 11. Open-load detection

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{OL}	Open-load on-state detection threshold	V_{IN} = 5V	35	70	140	mA
$t_{DOL(on)}$	Open-load on-state detection delay	I_{OUT} = 0A			200	µs
V_{OL}	Open-load off-state voltage detection threshold	V_{IN} = 0V	1.5	2.5	3.5	V
$t_{DOL(off)}$	Open-load detection delay at turn-off				1000	µs

Figure 4. Status timings

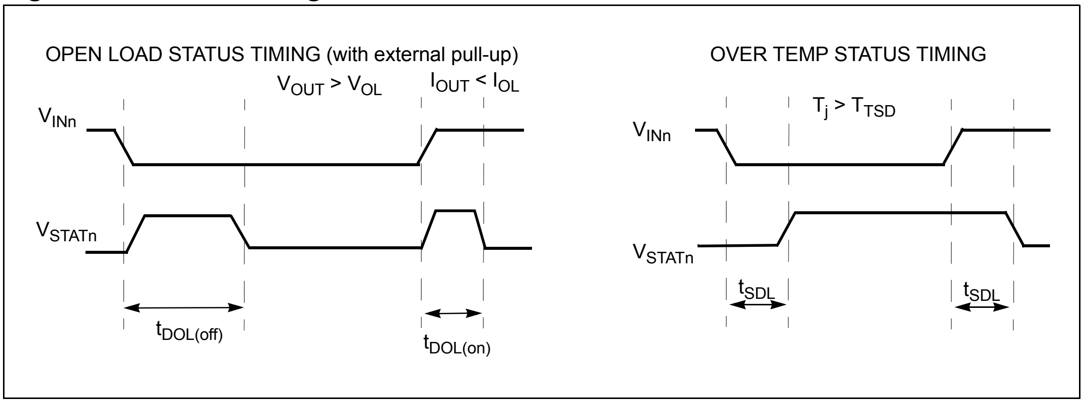


Figure 5. Switching characteristics

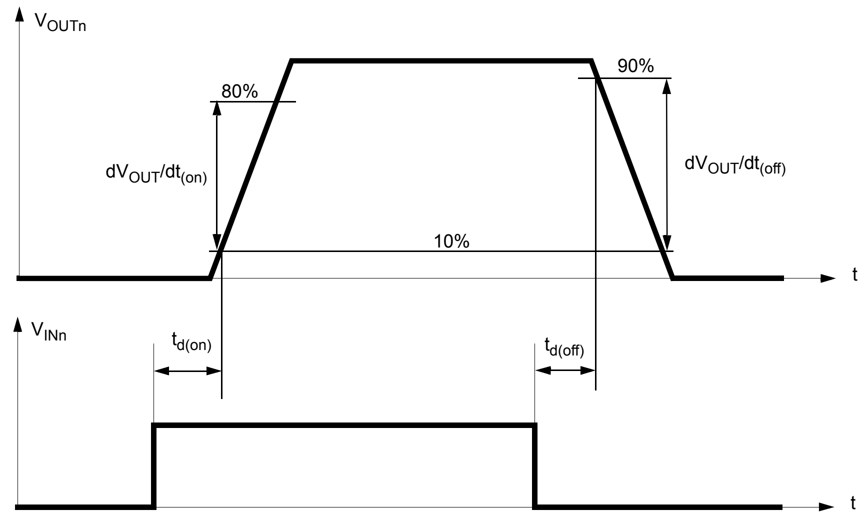


Table 12. Truth table

Conditions	Input	Output	Status
Normal operation	L H	L H	H H
Current limitation	L H H	L X X	H $(T_j < T_{TSD})$ H $(T_j > T_{TSD})$ L
Overtemperature	L H	L L	H L
Undervoltage	L H	L L	X X
Overvoltage	L H	L L	H H
Output voltage > V_{OL}	L H	H H	L H
Output current < I_{OL}	L H	L H	H L

Table 13. Electrical transient requirements (part 1/3)

ISO T/R 7637/1 Test pulse	Test level				
	I	II	III	IV	Delays and impedance
1	- 25V	- 50V	- 75V	- 100V	2ms, 10Ω
2	+ 25V	+ 50V	+ 75V	+ 100V	0.2ms, 10Ω
3a	- 25V	- 50V	- 100V	- 150V	0.1µs, 50Ω
3b	+ 25V	+ 50V	+ 75V	+ 100V	0.1µs, 50Ω
4	- 4V	- 5V	- 6V	- 7V	100ms, 0.01Ω
5	+ 26.5V	+ 46.5V	+ 66.5V	+ 86.5V	400ms, 2Ω

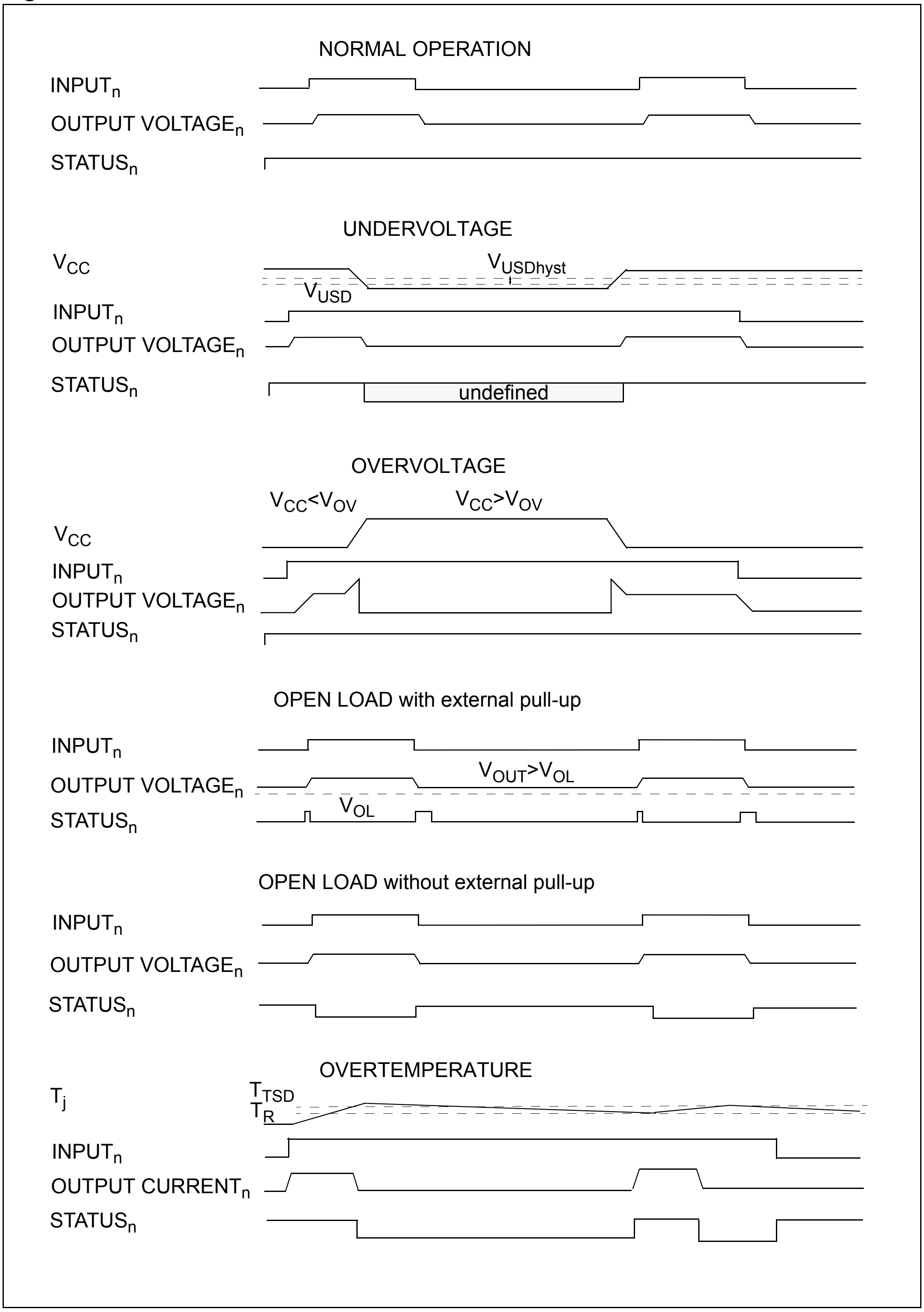
Table 14. Electrical transient requirements (part 2/3)

ISO T/R 7637/1 Test pulse	Test level			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

Table 15. Electrical transient requirements (part 3/3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device.

Figure 6. Waveforms



2.4 Electrical characteristics curves

Figure 7. Off-state output current

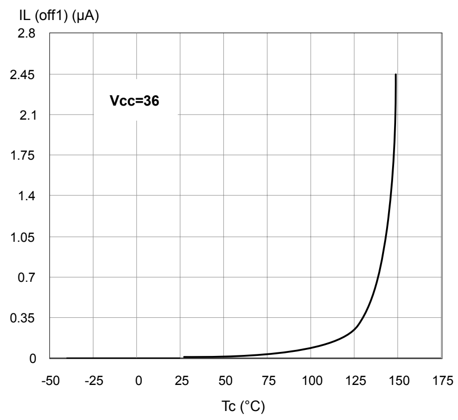


Figure 8. High level input current

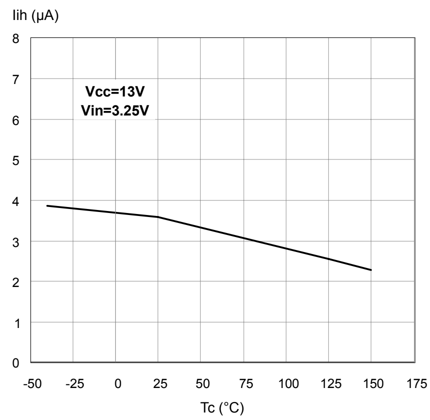


Figure 9. Input clamp voltage

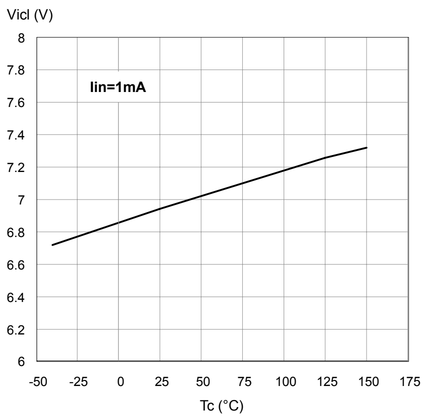


Figure 10. Turn-on voltage slope

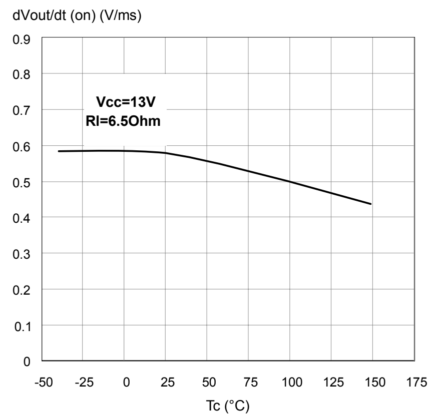


Figure 11. Overvoltage shutdown

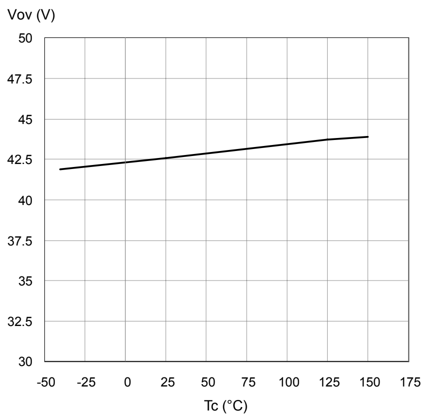


Figure 12. Turn-off voltage slope

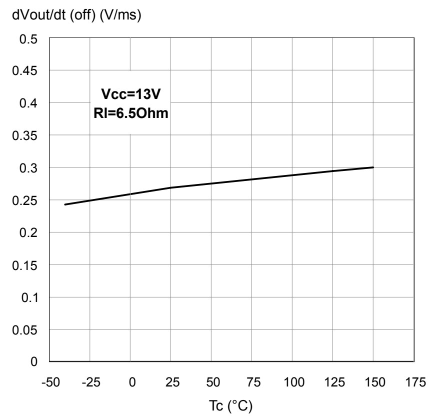


Figure 13. I_{LIM} vs T_{case}

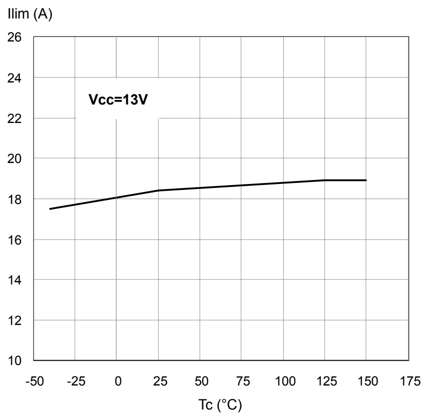


Figure 14. On-state resistance vs V_{CC}

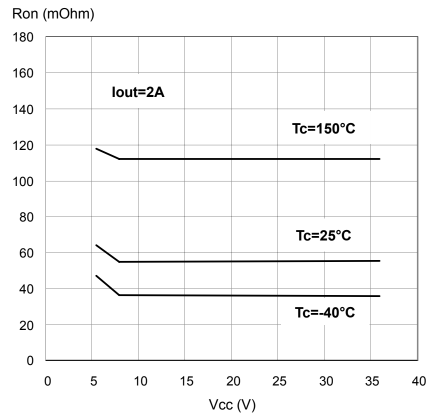


Figure 15. Input high level

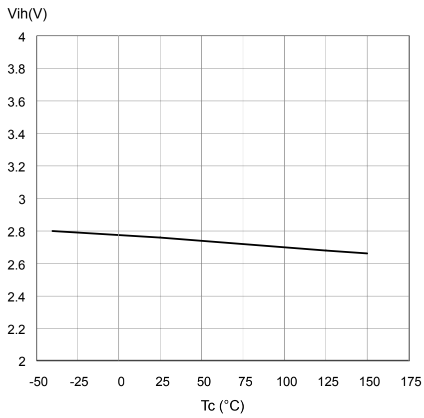


Figure 16. Input hysteresis voltage

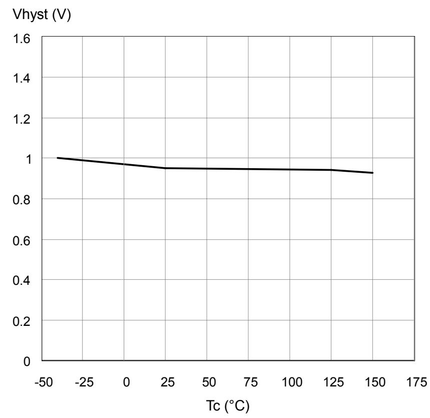


Figure 17. On-state resistance vs Tcase

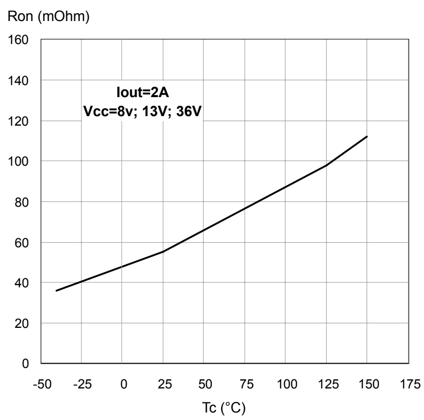


Figure 18. Input low level

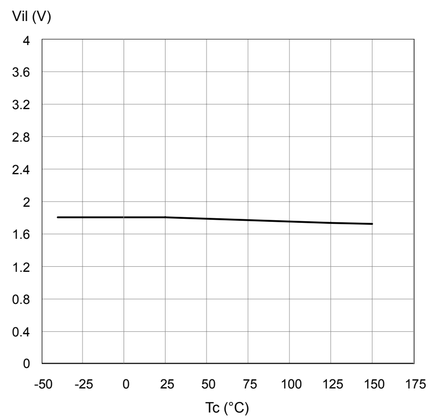


Figure 19. Status leakage current

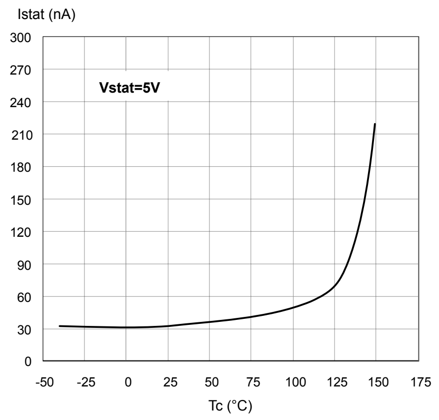


Figure 20. Status low output voltage

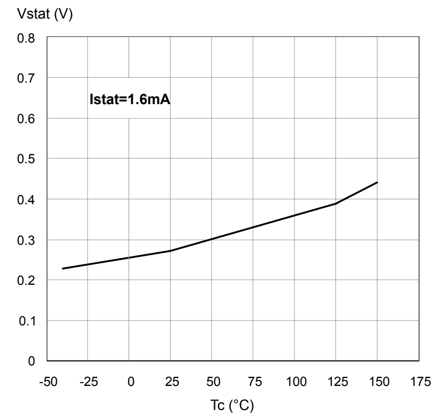


Figure 21. Status clamp voltage

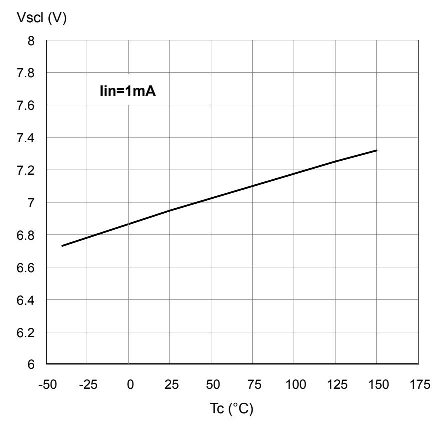


Figure 22. Open-load on-state detection threshold

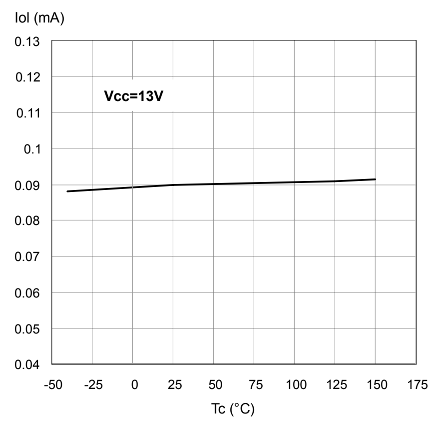
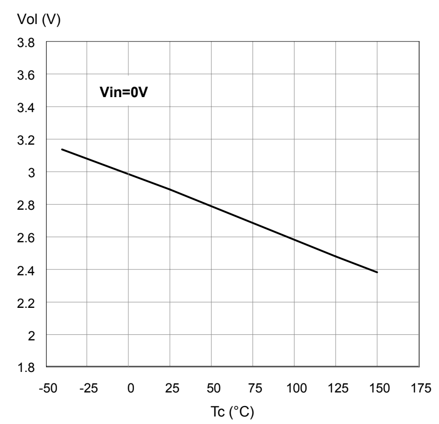
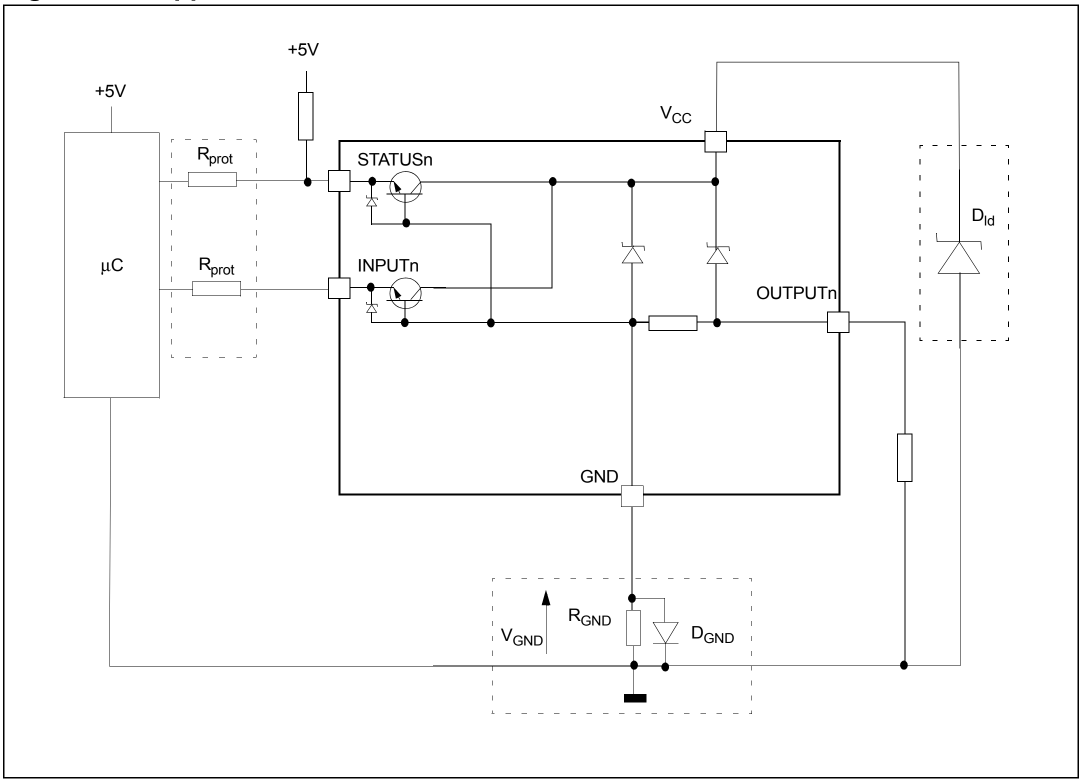


Figure 23. Open-load off-state voltage detection threshold



3 Application information

Figure 24. Application schematic



3.1 GND protection network against reverse battery

This section provides two solutions for implementing a ground protection network against reverse battery.

3.1.1 Solution 1: a resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following show how to dimension the R_{GND} resistor:

1. $R_{GND} \leq 600mV / 2 (I_{S(on)max})$
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in R_{GND} (when $V_{CC} < 0$ during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that, if the microprocessor ground is not shared by the device ground, then the R_{GND} will produce a shift ($I_{S(on)max}$ * R_{GND}) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation requires the use of a large resistor, or several devices have to share the same resistor, then ST suggests using solution 2 below.

3.1.2 Solution 2: a diode (D_{GND}) in the ground line

A resistor (R_{GND} = 1kΩ) should be inserted in parallel to D_{GND} if the device will be driving an inductive load. This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift (j600mV) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network. Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating. Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

3.2 Load dump protection

D_{ld} is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the V_{CC} maximum DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than those shown in the ISO T/R 7637/1 table.

3.3 MCU I/O protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the µC I/O pins from latching up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os:

$$- V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Example

For the following conditions:

V_{CCpeak} = - 100V

$I_{latchup} \geq$ 20mA

$V_{OH\mu C} \geq$ 4.5V

5kΩ ≤ R_{prot} ≤ 65kΩ.

Recommended values are:

R_{prot} = 10kΩ

3.4 Open-load detection in off-state

Off-state open load detection requires an external pull-up resistor (R_{PU}) connected between OUTPUT pin and a positive supply voltage (V_{PU}) like the +5V line used to supply the microprocessor.

The external resistor has to be selected according to the following requirements:

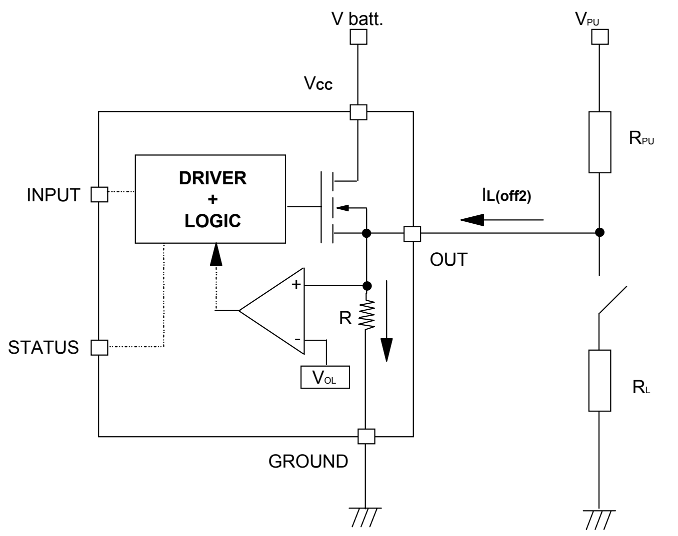
1) no false open load indication when load is connected: in this case we have to avoid V_{OUT} to be higher than V_{Olmin}; this results in the following condition

$V_{OUT} = (V_{PU} / (R_L + R_{PU}))R_L < V_{Olmin}$.

2) no misdetection when load is disconnected: in this case the V_{OUT} has to be higher than V_{OLmax}; this results in the following condition $R_{PU} < (V_{PU} - V_{OLmax}) / I_{L(off2)}$.

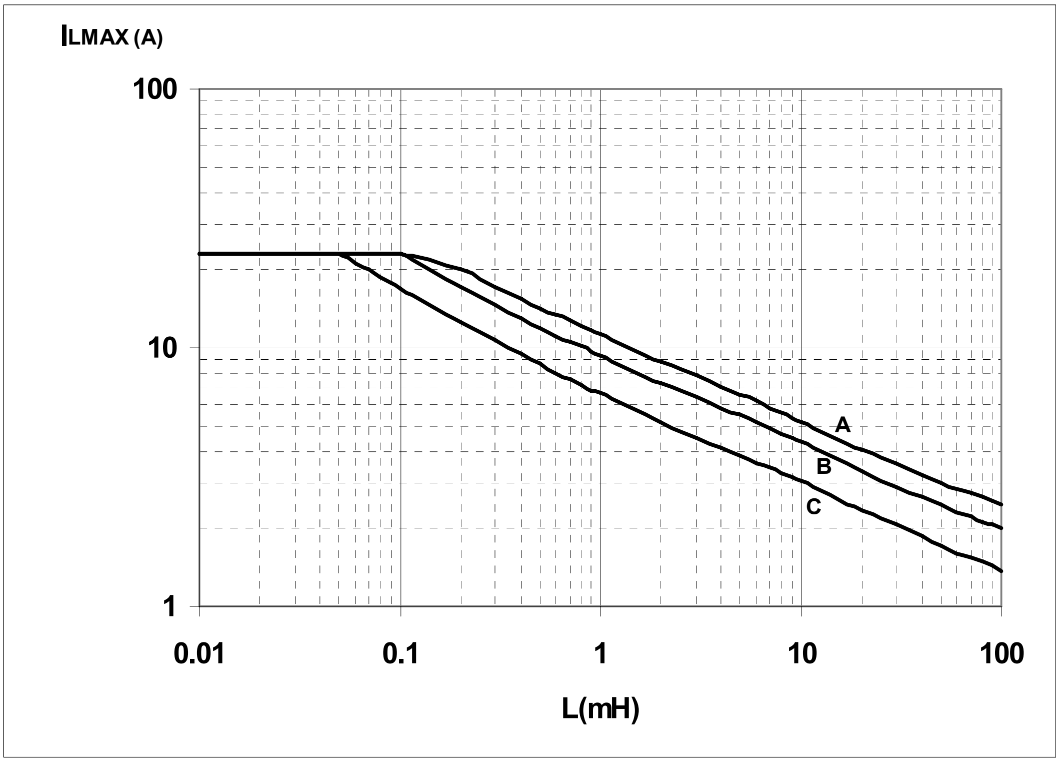
Because $I_{s(OFF)}$ may significantly increase if V_{out} is pulled high (up to several mA), the pull-up resistor R_{PU} should be connected to a supply that is switched OFF when the module is in standby.

Figure 25. Open-load detection in off-state



3.5 Maximum demagnetization energy (V_{CC} = 13.5V)

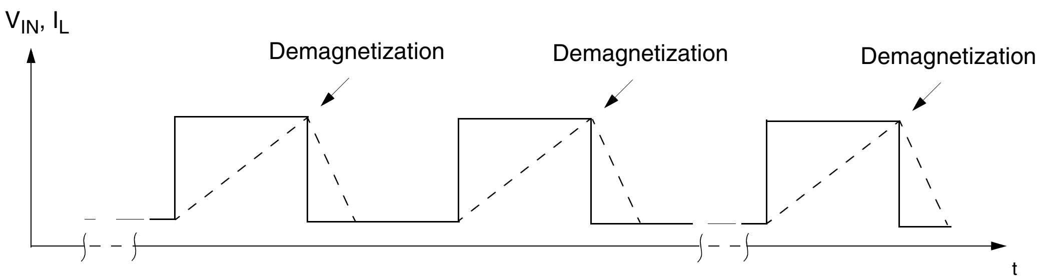
Figure 26. Maximum turn-off current versus load inductance



A = single pulse at T_{Jstart} = 150ºC

B= repetitive pulse at T_{Jstart} = 100ºC

C= repetitive pulse at T_{Jstart} = 125ºC

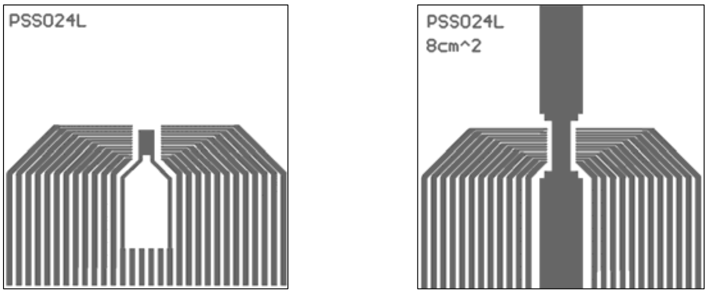


Note: *Values are generated with R_L = 0Ω.*
In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

4 Package and PC board thermal data

4.1 PowerSSO-24 thermal data

Figure 27. PowerSSO-24 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 78 mm x 78 mm, PCB thickness=2 mm, Cu thickness=70 mm (front and back side), Copper areas: from minimum pad lay-out to 8 cm^2).

Figure 28. $R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel ON)

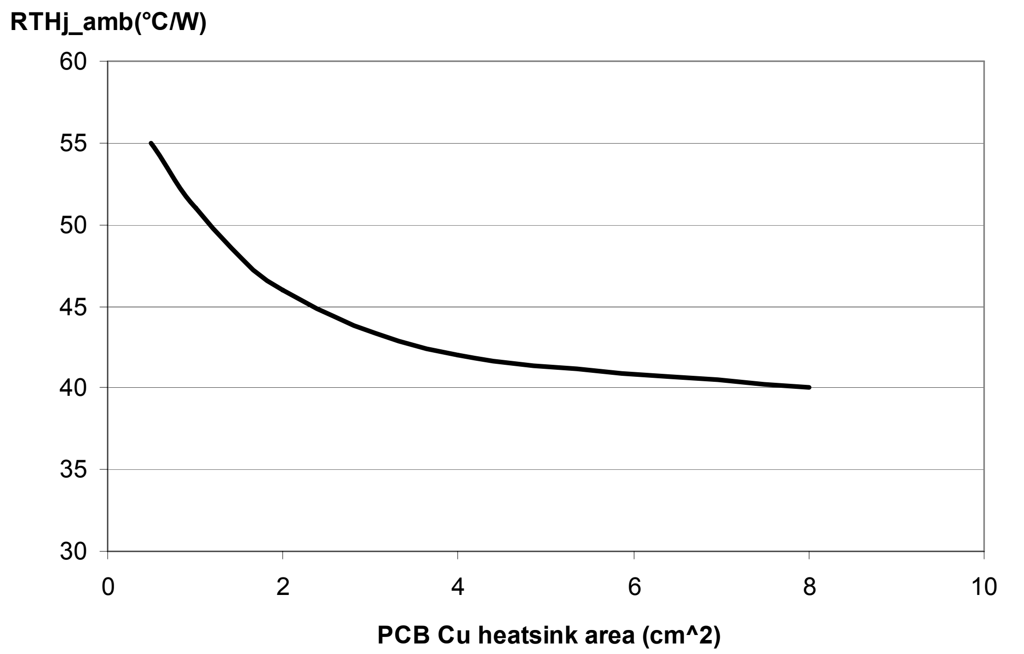


Figure 29. PowerSSO-24 thermal impedance junction ambient single pulse (one channel ON)

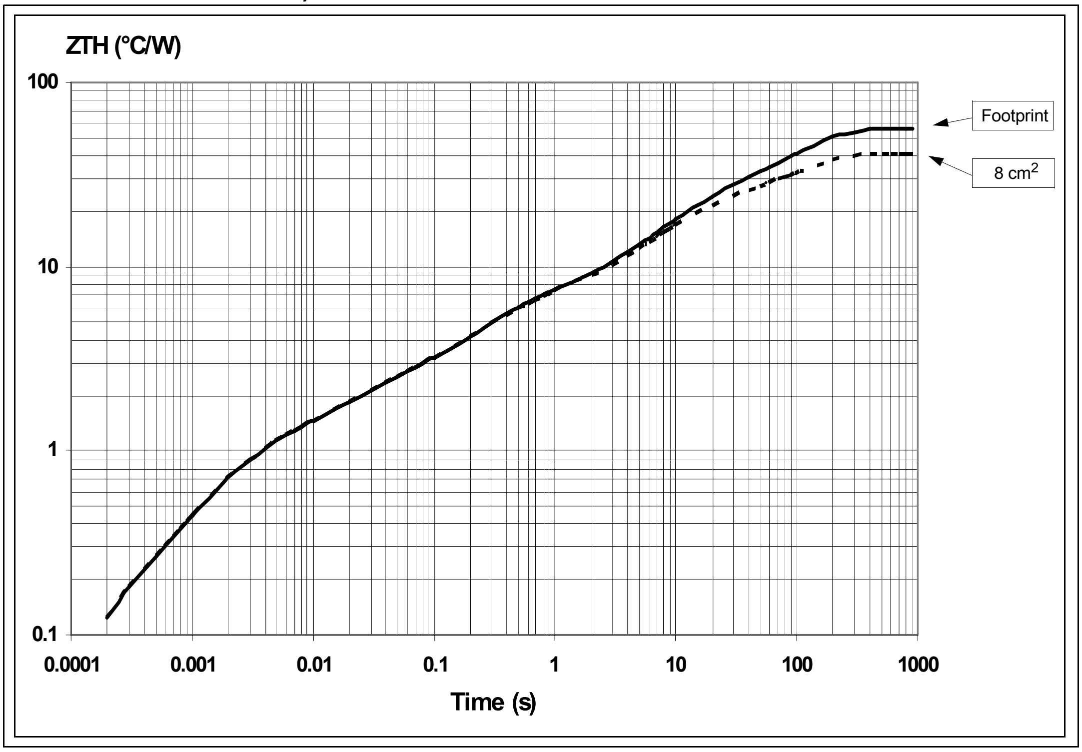
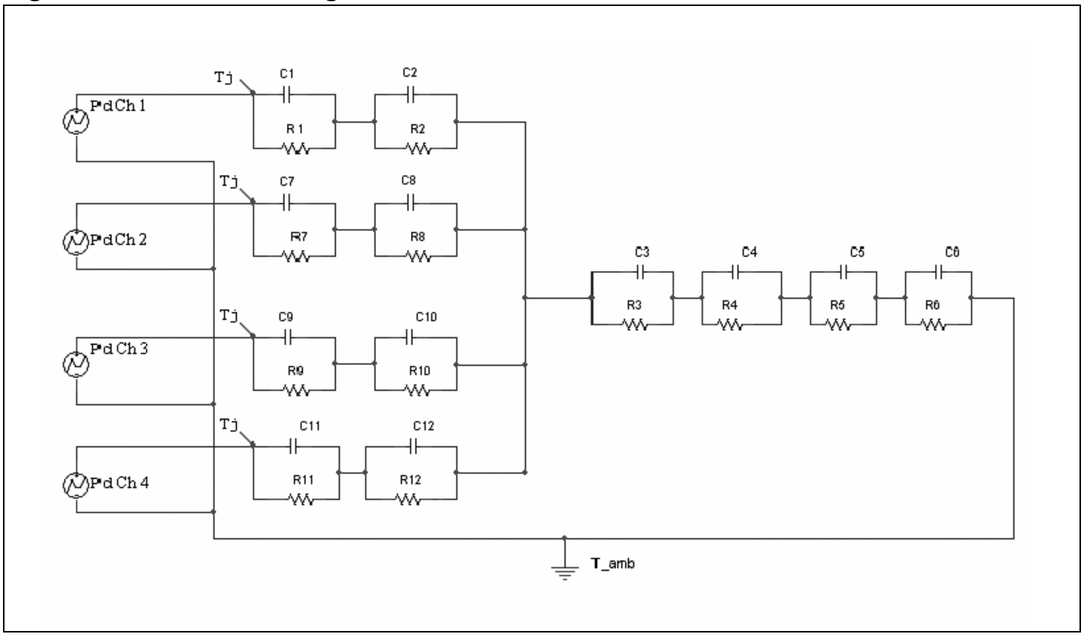


Figure 30. Thermal fitting model of a double channel HSD in PowerSSO-24 (b)



b. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Equation 1: pulse calculation formula:

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Table 16. Thermal parameters

Area/island (cm^2)	Footprint	8
R1 = R7 = R9 = R11 (°C/W)	0.1	
R2 = R8 = R10 = R12 (°C/W)	0.9	
R3 (°C/W)	1	
R4 (°C/W)	4	
R5 (°C/W)	13.5	
R6 (°C/W)	37	22
C1 = C7 = C9 = C11 (W.s/°C)	0.0006	
C2 = C8 = C10 = C12 (W.s/°C)	0.0025	
C3 (W.s/°C)	0.025	
C4 (W.s/°C)	0.08	
C5 (W.s/°C)	0.7	
C6 (W.s/°C)	3	5

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

5.2 PowerSSO-24 mechanical data

Figure 31. PowerSSO-24 package dimensions

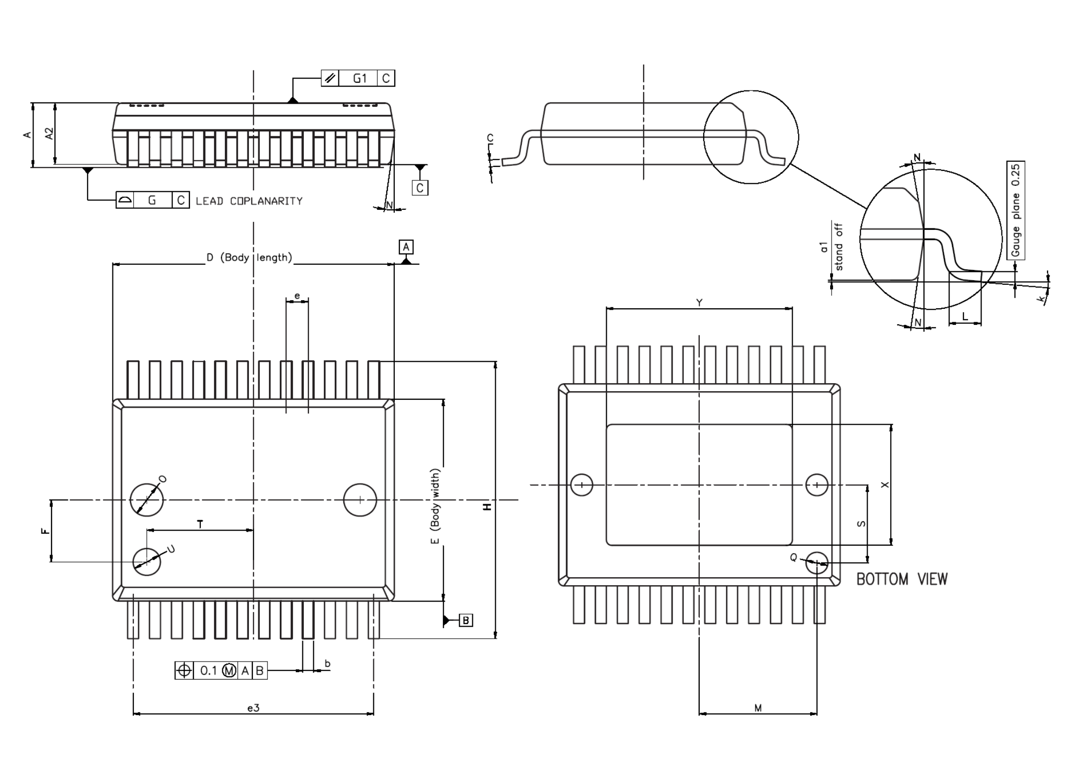


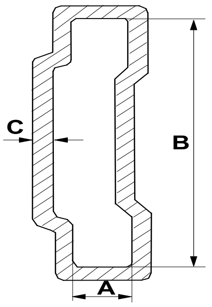
Table 17. PowerSSO-24 mechanical data[1] [2]

Symbol	Millimeters		
	Min.	Typ.	Max.
A			2.45
A2	2.15		2.35
a1	0		0.10
b	0.33		0.51
c	0.23		0.32
D[3]	10.10		10.50
E[3]	7.40		7.60
e		0.8	
e3		8.8	
F		2.3	
G			0.1
G1			0.06
H	10.1		10.5
h			0.4
k	0°		8°
L	0.55		0.85
O		1.2	
Q		0.8	
S		2.9	
T		3.65	
U		1	
N			10º
X	4.1		4.7
Y	6.5 4.9[4]		7.1 5.5[4]

1. No intrusion allowed inwards the leads.
2. Flash or bleeds on exposed die pad shall not exceed 0.4 mm per side
3. “D and E” do not include mold flash or protusions.
   Mold flash or protusions shall not exceed 0.15 mm.
4. Variations for small window lead frame option.

5.3 Packing information

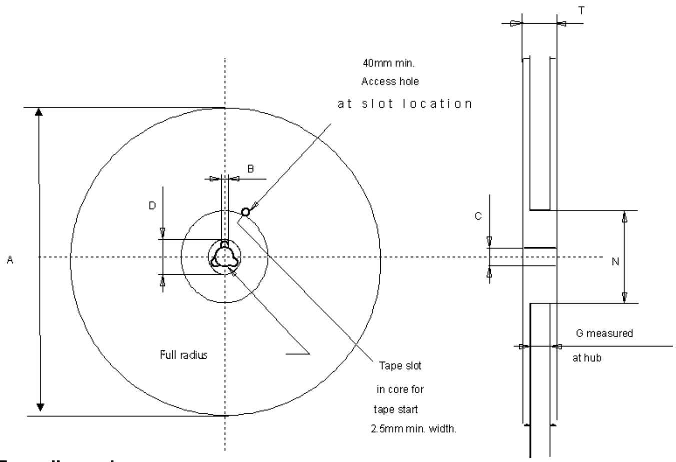
Figure 32. PowerSSO-24 tube shipment (no suffix)



Base Q.ty	49
Bulk Q.ty	1225
Tube length (± 0.5)	532
A	3.5
B	13.8
C (± 0.1)	0.6

All dimensions are in mm.

Figure 33. PowerSSO-24 tape and reel shipment (suffix “TR”)



Reel dimensions

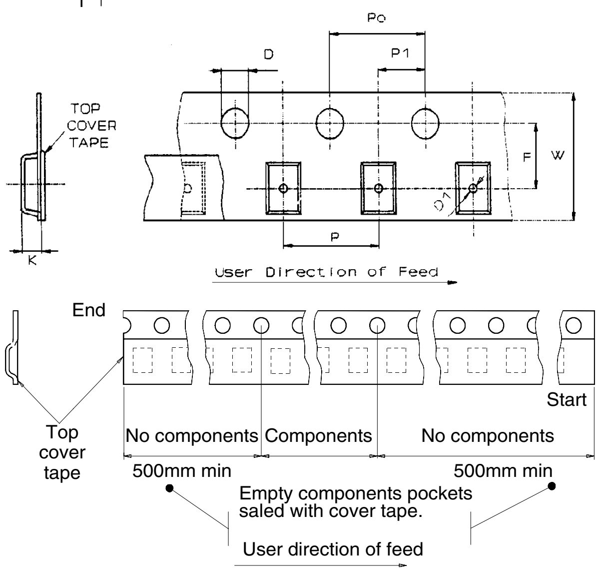
Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	100
T (max)	30.4

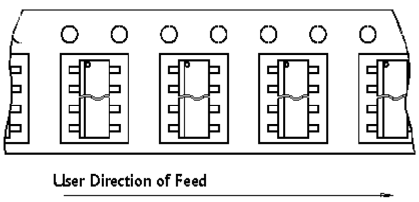
Tape dimensions

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	W	24
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	12
Hole Diameter	D (± 0.05)	1.55
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.1)	11.5
Compartment Depth	K (max)	2.85
Hole Spacing	P1 (± 0.1)	2

All dimensions are in mm.





6 Revision history

Table 18. Document revision history

Date	Revision	Changes
10-Nov-2004	1	Initial release.
22-Nov-2006	2	Pdf changed.
07-Dec-2004	3	Mechanical data updating. PowerSSO-24 thermal characterization insertion PCB copper area correction.
04-May-2005	4	Changed document status from preliminary to definitive.
03-May-2006	5	Configuration diagram modification Shipment data insertion
26-Nov-2008	6	Document reformatted and restructured. Added list of contents, tables and figures. Added *ECOPACK® packages* information. Update *PowerSSO-24 mechanical data*.
01-Jul-2009	7	*Table 17: PowerSSO-24 mechanical data*: – Deleted A (min) value – Changed A (max) value from 2.50 to 2.45 – Changed A2 (max) value from 2.40 to 2.35 – Updated k values – Changed L (min) value from 0.6 to 0.55 – Changed L (max) value from 1 to 0.85